ABSTRACT OF THE DISCLOSURE

Even when variation in transistor characteristic, resistance or the like occurs during manufacturing, a noise component is always minimized. Each of k clock phase difference generating circuits 16-18 shifts a phase of a basic clock signal ADCK1 by a specified different value to obtain a clock signal ADCK2 and supplies the clock signal ADCK 2 to an A/D converter. A k counter 19 successively selects the clock phase difference generating circuits 16-18 and stores a noise component in an output of the A/D converter measured by a noise measuring circuit 27 in a corresponding register. A comparator 25 compares k noise components and obtains the number j of the clock phase difference generating circuit giving a minimum value. A selection circuit 26 fixedly selects only the j-th clock phase difference generating circuit. Thus, even when variation in the transistor characteristics or resistance occurs in each device in a manufacturing stage, the clock signal ADCK2 obtained by shifting the phase of the basic clock signal ADCK1 can be supplied to the A/D converter so that a noise component is minimized for each device.